Dynamic Voltage and Frequency Scaling for Power-Constrained Design using Process Voltage and Temperature Sensor Circuits

Haiqing Nan*, Kyung Ki Kim*, Wei Wang* and Ken Choi*

Abstract—In deeply scaled CMOS technologies, two major non-ideal factors are threatening the survival of the CMOS; i) PVT (process, voltage, and temperature) variations and ii) leakage power consumption. In this paper, we propose a novel post-silicon tuning methodology to scale optimum voltage and frequency "dynamically". The proposed design technique will use our PVT sensor circuits to monitor the variations and based on the monitored variation data, voltage and frequency will be compensated "automatically". During the compensation process, supply voltage is dynamically adjusted to guarantee the minimum total power consumption without violating the frequency requirement. The simulation results show that the proposed technique can reduce the total power by 85% and the static power by 53% on average for the selected ISCAS'85 benchmark circuits with 45 nm CMOS technology compared to the results of the traditional PVT compensation method.

Keywords—PVT Variation sensors, Yield, Voltage Scaling, Frequency Scaling

1. INTRODUCTION

As technology scaling, especially below 65nm, manufactured dies expose large distribution range for their operation frequency and power consumption due to PVT variations [1]. Traditionally, the maximum operation frequency is the main factor to determine the yield of manufacture dies. However, during recent decades, power consumption has become an important factor for power-constrained designs which have very limited power supply budget [2-5]. Therefore, many dies which are fast but leaky will not satisfy the power constraint and will be discarded. Many dies which have slow speed due to their PVT variations are unable to meet the frequency requirement. Therefore, those slow dies are also discarded. To reduce the leakage power, power gating techniques are commonly used, which utilize on-off power switches inserted between the power supply rails and the circuit. While the circuit is in standby mode, the power switch is turned off and a significant amount of leakage power can be avoided. However, power gated circuits still suffer PVT variations. And it is still possible to violate the power constraint or frequency constraint for the circuit due to the PVT variations. Therefore, it is necessary to develop methodologies to reduce the impact of PVT variations on the performance as well as the power consumption of the circuits. Many researchers have proposed delay based [6] or temperature

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based [7] sensor circuits to monitor the performance of the system. According to the PVT variations of each die, different supply voltages or back biasing voltages are generated to compensate the performance degradation. The traditional method in the industry to compensate for the PVT variations is increasing the supply voltage to guarantee the slowest die (worst case) satisfying the frequency constraint. Therefore, all dies will satisfy the frequency constraint. However, this method has large power overhead and it is not feasible for power constrained designs. In this paper, we use our previous PVT sensor circuits proposed in [8] to reduce the power consumption of fast dies and increase the speed of slow dies dynamically. The fast but leaky dies which are supposed to be discarded due to their excessive power consumption, will have a relatively low supply voltage to reduce leakage power and dynamic power without violating the frequency constraint. The slow dies will have a relatively high supply of voltage in order to meet the frequency constraint. Therefore, those dies that are supposed to be discarded can be pulled back to an acceptable state considering both frequency constraints and power constraints thereby increasing the yield.

The remainder of this paper is organized as follows. In the next section, we will talk about the impact of PVT variations on VLSI circuits. In section 3, we will explain the PVT sensor circuits briefly and propose the PVT compensation methodology to dynamically scale the supply voltage and frequency to compensate for the PVT variations. In section 4, experiment results are presented using ISCAS'85 benchmark circuits and compared with the results using traditional methods. We draw conclusions in section 5.

2. RELATED WORK

Fig. 1 shows the impact of process variations and temperature variations on the performance of an inverter chain of 20 inverters, assuming the supply voltage is stable. We applied the process variations 300 times for the circuit. Three temperatures: 45°C, 50°C and 55°C are applied during the process variations. As it is shown in Fig. 1, the operating frequency of the circuit varies significantly according to the process variation and the temperature variation.

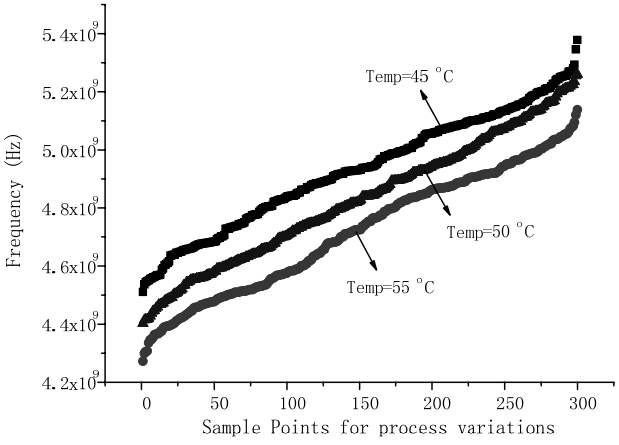

Fig. 1. Frequency variation due to PT variations

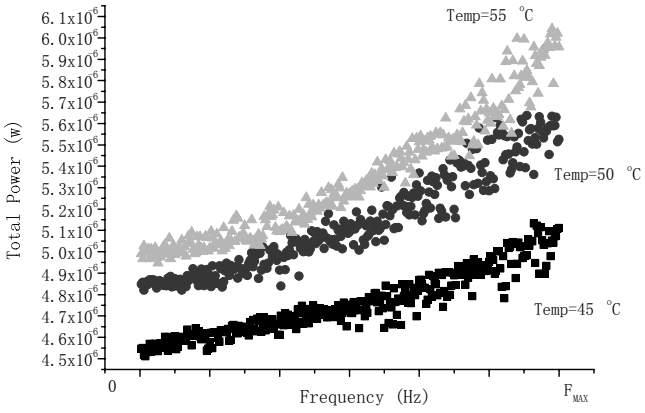

Fig. 2. Total power variation due to PT variation

Fig. 2 shows the total power variation (dynamic power + static power) due to the PT variations. The total power increases with the increase of the frequency and temperature. Due to the frequency and power variations, many fast but leaky dies may violate the power constraint or frequency constraint. Therefore, it is necessary to design a system with PVT variation monitoring and compensation capability to reduce high power consumption or increase the low operating frequency of manufactured dies due to the PVT variations.

3. IMPACT OF PVT VARIATIONS ON VLSI CIRCUITS

We take advantage of our previous PVT monitoring circuits and propose a dynamic voltage and frequency scaling methodology to compensate for the impact of PVT variations. Fig. 3 shows the PVT sensor circuits from [8] including a temperature sensor, a process sensor and a power supply noise compensator. The temperature sensor and process sensor generate output voltages proportional to the temperature and process. Two A/D converters are used to convert the analog output voltages from the temperature sensor and the process sensor to three bit digital signals. T1, T2 and T3 represent the temperatures 45°C, 50°C and 55°C. P1, P2 and P3 represent the process corners slow, typical and fast. The supply voltage look up table is constructed before hand through extensive simulation of the DUT to achieve the minimum power consumption without violating the frequency constraint. The supply voltage from the look up table is connected with the power supply noise compensation circuit to provide a stable and noise immune voltage to the DUT. Due to lack of the paper space, we omitted the details of the circuit explanations.

For the system on chip (SoC) design, many power domains are partitioned on the chip. Each power domain has its specified supply voltage. Due to the PVT variations, the power domains suffer severe frequency and power variations. Therefore, many manufactured dies may not satisfy the power constraint or the frequency constraint. However, if the PVT sensor circuits are integrated with each power domain to monitor and compensate the PVT variations, the power consumption of the dies can be reduced to an acceptable range, and the frequency of the dies can be adjusted to meet the frequency constraint.

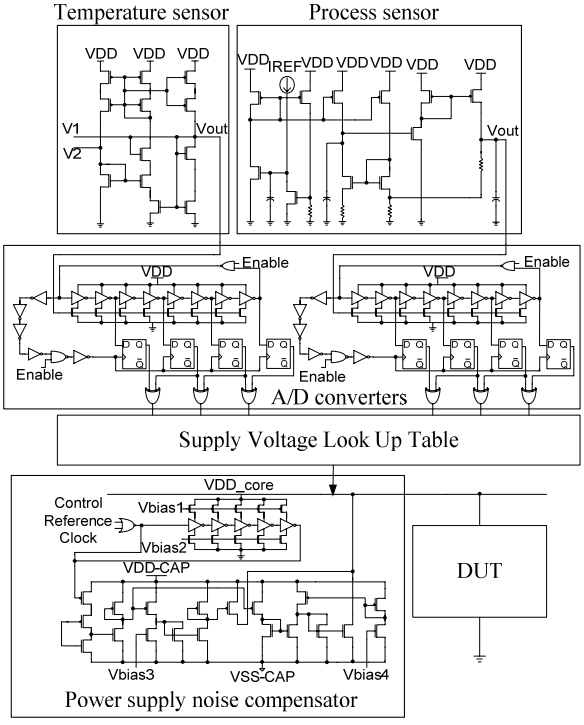

Fig. 3. PVT sensor circuits and compensation method [8]

Fig.4 shows a SoC design with six power domains. Each power domain has its own supply-voltage. The PVT sensors are integrated with each power domain to monitor the PVT variations. According to the PVT variations, the different supply voltage will be generated for the power domain through the look up table circuit. Different power domains have different look up tables.

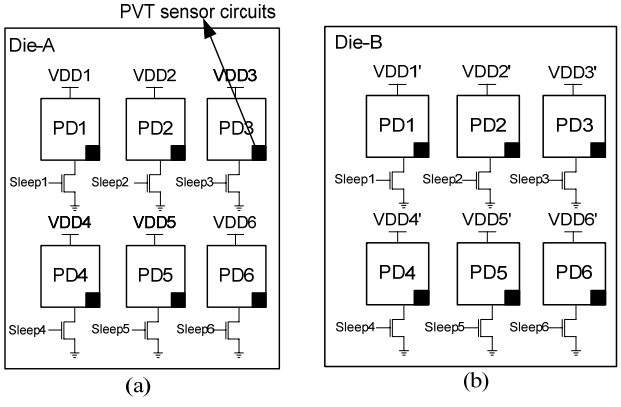

Fig. 4. SoC integrated with PVT sensors under PVT variation 1 (a), and PVT variation2 (b)

However, the same power domains in the different dies have the same look up table. For example, the power domain 1 (PD1) in die-A and die-B of Fig. 4 suffer different PVT variations and different supply voltages (VDD1 for PD1 of die-A and VDD1' for PD1 of die-B) are generated to compensate for the PVT variations. The PD1 in die-A and the PD1 in die-B have the same supply voltage look up table circuit.

4. EXPERIMENT RESULTS

In order to prove the effectiveness of the proposed methodology to compensate for the impact of the PVT variations on power and frequency, the selected ISCAS'85 benchmark circuits were simulated using 45nm PTM model [9] with power gating structure at supply voltage 1V. Power gating switches were inserted for each selected benchmark circuit to reduce the static power. All the simulation results and comparison results were based on the benchmark circuits with power gating switches. The traditional method to compensate for the PVT variations is using higher global supply voltage to guarantee the slowest die (worst case) satisfying the frequency constraint. The constrained frequency is defined as the frequency of the circuit when it operates at 50°C with typical process corner.

The selected ISCAS'85 benchmark circuits were simulated at three temperature conditions (T1: 45°C, T2: 50°C, and T3: 55°C) and three process corners (P1: slow, P2: typical, and P3: fast). Fig. 5 shows the performance comparison between the proposed PVT compensation method and traditional PVT compensation method in terms of frequency variation compensation, total power consumption, and static power consumption for ISCAS'85 C432 and C6288 circuits.

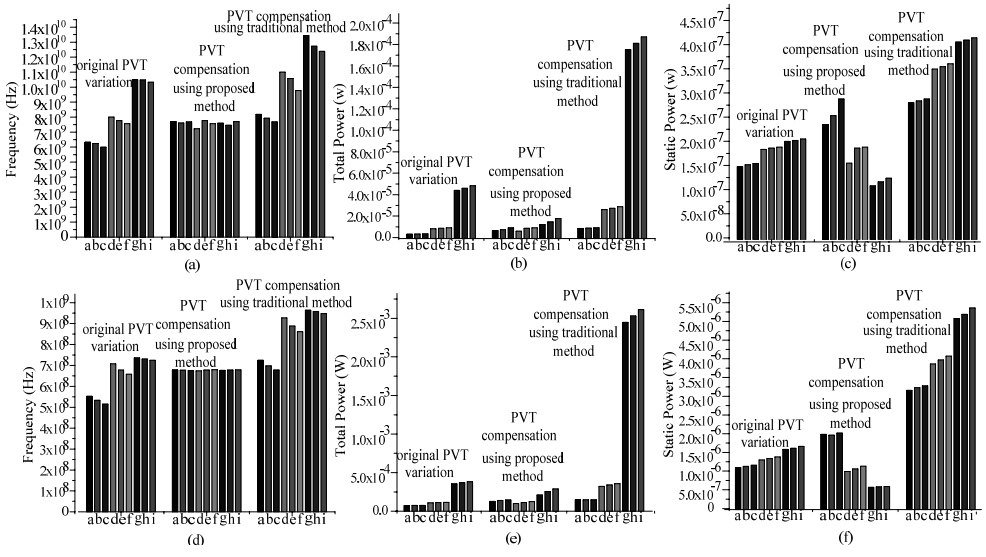

Fig. 5. PT variation compensation for C432 and C6288 using proposed and traditional methods for nine PT corners. (a) Frequency compensation for C432, (b) total power consumption for C432, (c) static power consumption for C432, (d) frequency compensation for C6288, (e) total power consumption for C6288, (f) static power consumption (a: P1T1, b: P1T2, c: P1T3, d: P2T1, e: P2T2, f: P2T3, g: P3T1, h: P3T2, i: P3T3)

Table 1. Supply Voltage Lookup Table for ISCAS'85 C1908 Circuit

T1	T2	T3	P1	P2	P3	Supply Voltage	Voltage Level
1	0	0	1	0	0	1.2V	V2
0	1	0	1	0	0	1.24V	V1
0	0	1	1	0	0	1.24V	V1
1	0	0	0	1	0	0.98V	V4
0	1	0	0	1	0	1.00V	V3
0	0	1	0	1	0	1.00V	V3
1	0	0	0	0	1	0.78V	V5
0	1	0	0	0	1	0.78V	V5
0	0	1	0	0	1	0.78V	V5

Fig. 5 (a) and Fig. 5 (d) show that both the proposed method and traditional method can guarantee the frequency constraint for all PT variation corners. However, according to Fig. 5 (b) (c) (e) (f), the proposed method saves huge amounts of dynamic power and static power compared to the traditional method.

Table 1 shows the supply voltage look up table for the ISCAS'85 C1908 circuit. The supply voltages were selected through extensive simulation to minimize the total power consumption without violating the frequency constraint. The supply voltage look up table circuit of C1908 is shown in Fig. 6. According to the output of the A/D converters, which represent the temperature and process corners, the look up table circuit selects one of the voltages from V1 to V5. The look up table circuit consists of a resistor tree, pass transistors, and a voltage regulator. The resistor tree consists of six resistors connected in serial, which divides the voltage between the output of the opamp and ground into five different voltages, which are used as the supply voltages of the circuit according to different PVT variation scenarios without violating the frequency constraint. The supply voltage look up table circuit of the C1908 is shown in Fig. 6. According to the output of the A/D converters, which represent the temperature and process cor-

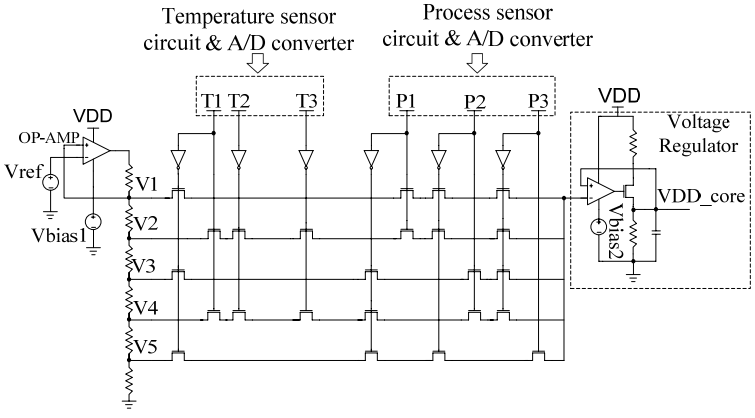

Fig. 6. Supply voltage look up table circuit for C1908

ners, the look up table circuit selects one of the voltages from V1 to V5. The look up table circuit consists of a resistor tree, pass transistors, and a voltage regulator. The resistor tree consists of six resistors connected in serial, which divides the voltage between the output of the opamp and ground into five different voltages, which are used as the supply voltages of the circuit according to different PVT variation scenarios.

Table 2 shows the simulation results for the selected ISCAS'85 benchmark circuits. The results show that both the proposed PVT compensation method and the traditional PVT compensation method can guarantee the frequency constraint for the selected benchmark circuits. Moreover, the proposed method reduces total power 85% on average and static power 53% on average compared to the traditional method for the selected ISCAS'85 benchmark circuits, due to the fact that the voltage supply is dynamically adjusted according to the PVT variations.

Fig. 7 shows the layout of the ISCAS'85 C6288 circuit with the on chip PVT sensor circuits.

Table 2. Performance Comparison Between the Traditional PVT Compensation Method & Proposed PVT Compensation Method

Circuit	# of TR	Traditional Method				Proposed Method (dynamic PVT compensation)					Power Saving	
		Compensated Vdd	Frequency Constrain Meet	Total Power (W) (average)	Static Power (W) (average)	Compensated Vdd Dynamically (average)		Frequency Constrain Meet	Total Power (W) (average)	Static Power (W) (average)	Total Power	Static Power
C432	878	1.22V	Yes	7.54E-05	3.78E-07	0.99 V	min:0.8V max:1.22V	Yes	1.13E-05	2.00E-07	85%	47%
C499	2980	1.28V	Yes	2.33E-04	1.25E-06	1.02V	min:0.82V max:1.28V	Yes	2.69E-05	5.15E-07	88%	58%
C1908	3786	1.24V	Yes	2.97E-04	1.02E-06	1.01V	min:0.8V max:1.24V	Yes	3.40E-05	5.42E-07	88%	46%
C5315	12346	1.26V	Yes	6.42E-04	3.99E-06	1.02V	min:0.8V max:1.26V	Yes	1.10E-04	2.23E-06	83%	44%
C6288	10112	1.25V	Yes	1.01E-03	4.14E-06	1.02V	min:0.8V max:1.25V	Yes	1.67E-04	1.23E-06	83%	70%

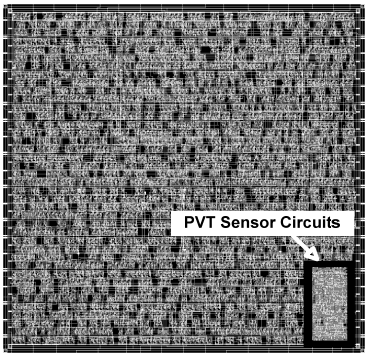

Fig. 7. Layout of C6288 circuit integrated with PVT sensors,
Size of sensor circuits: width=6.13um, height=13.5um,
Total size with C6288 and sensors: width=42.17um, height=48.26um

The area overhead due to the PVT sensor circuits is 4%. The power overhead due to the PVT sensors is 141uw.

5. CONCLUSION

In this paper, we propose a new methodology to dynamically scale the supply voltage and frequency for the power-constrained SoC design, considering PVT variations. PVT monitoring circuits are integrated with each power domain to monitor the on-chip variations. Based on the monitored variation data, voltage and frequency will be compensated for automatically. The compensation for supply voltage is dynamically adjusted to guarantee the minimum total power consumption without violating the frequency specification. The simulation results show that the proposed technique can reduce the total power by 85% and the static power by 53% on average for the ISCAS'85 benchmark circuits with 45 nm CMOS technology compared to the results of the traditional PVT compensation method.

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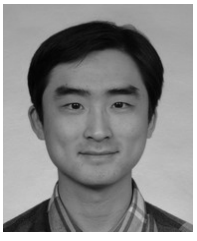

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